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the pad terminal communicating an electrical signal to an outer device and the terminal of the outer device cohere well with each other, and to the structure of an LCD having the same pad terminal.

Please replace the paragraph beginning at page 2, line 20, with the following rewritten paragraph:

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The lower panel 5 of the LCD comprises switching elements and bus lines generating the electric field for driving the liquid crystal layer. This panel is called an active panel. The active panel 5 of an AMLCD includes pixel electrodes 41 designed in a matrix pattern and formed on a second transparent substrate1b. Along the column direction of the pixel electrodes 41, signal bus lines 13 are formed, and along the row direction of the pixel electrodes 41, data bus lines 23 are formed. At a corner of a pixel electrode 41, a TFT 19 for driving the pixel electrode 41 is formed. A gate electrode 11 of the TFT 19 is connected with the signal bus line 13 (or the gate line). A source electrode 21 of the TFT 19 is connected with the data line 23 (or the source line). A semiconductor layer 33 is formed between the source electrode 21 and the drain electrode 31. An ohmic contact exists between the source electrode 21 and the semiconductor layer 33 and between the drain electrode 31 and the semiconductor layer 33 are also ohmic contacted. A gate pad 15 and a source pad 67, the terminals of the bus lines, are formed at the end portion of the gate line 13 and the source line 23, respectively. Additionally, a gate pad terminal 57 and a source pad terminal 25 are formed on the gate pad 15 and the source pad 67, respectively.

Please replace the paragraph beginning at page 3, line 15, with the following rewritten paragraph:

As the signal voltage applied to the gate pad 15 is applied to the gate electrode 11 via the gate line 13, the TFT 19 of the corresponding gate electrode 11 transitions to the ON state. Then

the source electrode 21 and the drain electrode 31 of the TFT 19 are electrically connected so that the electrical picture data applied to the source pad 25 is sent to the drain electrode 31 through the source line 23 and the source electrode 21. Therefore, by controlling the signal voltage to the gate electrode 11, the transfer of picture data to the drain electrode is controlled. That is, the TFT 19 acts as a switching element. A gate insulating layer 17 is inserted between the layer including the gate electrode 11 and the layer including the source electrode 23 to electrically isolate them. A passivation layer 37 is formed on the layer including the source line 23 to protect all elements of the transistor.

Please replace the paragraph beginning at page 4, line 18, with the following rewritten paragraph:

As shown in Fig. 3, the ACF 71 comprises a plurality of conductive ball 95 coated with an insulation membrane 93 in an isotropic film 31. On the pad terminals 47 connected to the pads 45 (for example, the gate pads 15 or the source pad 67) at the edge of the liquid crystal panel, an ACF 71 is attached and TCP 73 is sequentially attached thereon. At this time, the conductive pad 75 of the TCP 73 should be aligned with the pad 45 (for example, the gate pads 15 or the source pad 67) of the liquid crystal panel, as shown in Fig. 4a. The TCP 73 is pressed and heated while the conductive balls 95 are inserted between the TCP pad 75 and the pad terminal 47 of the liquid crystal panel. When sufficient pressure is applied against the TCP 73, the insulation membrane 93 covering the conductive ball 95 are broken so that each TCP pad 75 becomes electrically connected to each pad terminal 47 of the liquid crystal panel, as shown in Fig. 4b. Even if there are some conductive balls 95 between the neighbored pad terminals 47, the neighbored pad terminals 47 are electrically isolated from each other because the conductive balls 95 are covered by the insulation membrane 93.

Please replace the paragraph beginning at page 9, line 2, with the following rewritten paragraph:

Fig. 7 shows a plan view of an active panel according to a preferred embodiment of the present invention. On a transparent substrate 101, a first metal layer 211 is formed by depositing aluminum or aluminum alloy, as shown in Fig. 8a. A second metal layer 213 is formed by depositing a metal having a high melting point such as molybdenum, tantalum, tungsten or antimony sequentially on the first metal layer 211. These stacked metal layers 211 and 213 are patterned in a first mask process to form a gate electrode 111, a gate line 113 and a gate pad 115. Once these stacked layers 211 and 213 are patterned by a wet etching method, then the gate materials, such as the gate electrode, the gate line and the gate pad have a cross sectional shape where the width of the second metal layer 213 is narrower than that of the first metal layer 211. A plurality of the gate lines 113 is arrayed and fabricated in a vertical direction. The gate electrode 111 is derived from the gate line 113 and disposed at a corner of the designed pixel. The gate pad 115 is disposed at the end of the gate line 113, as shown in Figs. 7 and 8a.

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Please replace the paragraph beginning at page 9, lines 20 with the following rewritten paragraph:

On the substrate having the gate material stacked with the first metal layer_211 and the second metal layer 213, an inorganic insulating material such as a silicon nitride or a silicon oxide or an organic insulating material such as BCB (benzocyclobutane) or acrylic resin is coated to form a gate 5 insulating layer 117. An intrinsic semiconductor material, such as a pure amorphous silicon, and an extrinsic semiconductor material, such as an impurity doped amorphous silicon, are sequentially deposited thereon. These stacked layers are patterned using a second mask process to form a semiconductor layer 133 and a doped semiconductor layer 135.